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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,469	03/11/2004	Yun-Sang Lee	SAM-0536	6116

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Steven M. Mills
MILLS & ONELLO LLP
Suite 605
Eleven Beacon Street
Boston, MA 02108

EXAMINER	
NGUYEN, VAN THU T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,469	LEE ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8,10-12,14,15 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-6,19 and 20* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *10,18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 02/21/2006 has been entered and considered.

2. Claims 1-6, 8, 10-12, 14-15, 17-20 are pending.

3. Claims 17-20 are newly added.

4. After reconsideration, some of the allowable subject matters cited in Office Action filed on 11/14/2005 are withdrawn. A new Office Action is as follow.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims **1-3, 11-12** are rejected under 35 U.S.C. 102(e) as being anticipated by Ooishi, U.S. Patent No. 6,519,192 (Ooishi).

Regarding claim 1, Ooishi discloses a semiconductor memory device comprising:

a memory cell array (memory cell array 50, see FIGS. 1-2) including a plurality of memory cells connected between a plurality of word lines (e.g. subword line SWL, see FIG. 2) and a plurality of bit line pairs (e.g. BL and /BL, see FIG. 4);

a predetermined number of write line pairs (e.g. normal write data line pair NWDB and /NWDB, see FIG. 4 and column 7, lines 27-32);

a predetermined number of read line pairs (e.g. normal read data line pair NRDB and /NRDB, see FIG. 4 and column 7, lines 27-32);

a data input circuit for transmitting first data which is applied through data input pads to the predetermined number of write line pairs as second data during a write operation (I/O terminals connected to data bus portion for transmitting write data, wherein data at I/O terminals being considered as first data and data after transmitted on NWDB and /NWDB being considered as second data, see FIG. 1-2, and column 7 lines 56-60 and column 8 lines 3-5);

a plurality of write column selection gates for transmitting data between the plurality of bit line pairs and the predetermined number of write line pairs during a write operation (transistors 2020 and 2022, see FIG. 4 and column 10 lines 57 to column 11 line 3); and

a plurality of read column selection gates for transmitting data between the plurality of bit line pairs and the predetermined number of read line pairs in response to a read operation (transistors 2010 and 2012, see FIG. 4 and column 11 lines 4-9);

a data output circuit for outputting the third data as fourth data during the read operation, wherein the fourth data is output through data output pads (I/O terminals connected to data bus portion for transmitting read data, wherein data transmitted on NRDB and /NRDB being considered as third data and data at I/O terminals after being transmitted being considered as fourth data, see FIG. 1-2, and column 7 lines 56-60 and column 8 lines 3-5), and wherein the first data is

input through the data input pads during the write operation and the fourth data is output through the data output pads during the read operation simultaneously (see column 6, lines 39-47, and column 16 lines 57-61).

Regarding claims 2-3, Ooishi discloses a command decoder for decoding externally input command signals and generating a write command for the write operation and a read command for the read operation simultaneously (control circuit 20, see FIG. 1, and column 6 lines 1-8).

Regarding claims 11-12, they encompass the same scope of invention as to that of claims 1-3 except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims **8, 14-15, 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka, U.S. Patent No. 6,542,428 (Hikada) in view of Ooishi.

Regarding claim 8, Hidaka discloses a semiconductor memory device comprising:

a memory cell array (101, see FIG. 2) including a plurality of memory cell array blocks (110, see FIG. 2) each including a plurality of inherently memory cells connected between a plurality of inherent word lines and a plurality of bit line pairs (e.g. BL1-/BL1 to BL4-/BL4, see FIG. 6);

a predetermined number of local write line pairs of each of the plurality of memory cell array blocks for inputting data in each of the plurality of memory cell array blocks (local write line pair LW1 and /LW1 for each block 110, see FIG. 6);

a predetermined number of local read line pairs of each of the plurality of memory cell array blocks for outputting data of each of the plurality of memory cell array blocks (local read line pair LR0 and /LR0 for each block 110, see FIG. 6);

a plurality of write column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local write line pairs during a write operation (write column select gates WCSG1-WCSG4);

read column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local read line pairs during a read operation (read column select gate RGT1-RGT4);

a predetermined number of global write line pairs connected to a predetermined number of local write line pairs of each of the plurality of memory cell array blocks (a global write data bus pair GWDB and /GWDB for memory cell array blocks along one column, see FIGS. 2 and 6)

a predetermined number of global read line pairs connected to a predetermined number of local read line pairs of each of the plurality of memory cell array blocks (a global read data bus pair GRDB and /GRDB for memory cell array blocks along one column, see FIGS. 2 and 6);

a data input circuit for transmitting data input from a predetermined number of data input pads to the predetermined number of global write line pairs (part of I/O buffer circuit 85 connected to Din);

a data output circuit for outputting data transmitted from the predetermined number of global read line pairs to a predetermined number of data output pads (part of I/O buffer circuit 85 connected to Dout);

a command decoder for decoding externally input command signals and generating a write command for the write operation and a read instruction for the read operation (control circuit 26 receiving external input command signals /RAS, /CAS, /WE and generating inherent read/write command for read/write operations, see FIG. 1).

However, Hikada does not discloses that the command decoder generates write and read commands for performing write and read operations simultaneously.

Ooishi discloses a command decoder for decoding externally input command signals and generating a write command for the write operation and a read command for the read operation simultaneously (control circuit 20, see FIG. 1, and column 6 lines 1-8).

Since Hidaka and Ooishi are both from the same field of endeavor, the purpose disclosed by Ooishi would have been recognized in the pertinent art of Hidaka.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the concept of simultaneous read and write operations in a memory device disclosed in Hidaka for the purpose of simultaneously handling large volumes of data.

Regarding claims 14-15, they encompass the same scope of invention as to that of claim 8 except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Regarding claim 17, it is rejected under U.S.C 103(a) since it recites the same limitations as in claim 8.

Allowable Subject Matter

9. Claims **4-6, 19-20** are allowed.

10. Claims **10, 18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowability:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Hidaka and Ooishi, taken individually or in combination, do not teach the claimed invention having the following limitations, in combination with the remaining claimed limitations:

As in claim 10, 18: a first switch for transmitting data input to a predetermined number of data input pads to the data input circuit in response to a control signal, and transmitting data transmitted from the data output circuit to a predetermined number of data output pads; and a second switch for transmitting data input through the predetermined number of data output pads to the data input circuit in response to an inverted signal of the control signal, and transmitting data output from the data output circuit to the predetermined number of data input pads.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300..

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 18, 2006

VanThu Nguyen
Primary Examiner
Art Unit 2824